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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/704,467 | 10/31/2000 | Charles P. Roth | 10559-286001 | 5582 |

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| EXAMINER |
|---|
| LI, AIMEE J |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | 4 |

DATE MAILED: 09/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/704,467 | ROTH ET AL. | |
| | Examiner | Art Unit | |
| | Aimee J Li | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *31 October 2000 and 27 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

1. Claims 1-23 have been considered.

### *Papers Submitted*

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Change of Address as received on 16 December 2002 and IDS as received on 27 May 2003.

### *Drawings*

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Figure 4, element 400. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Specification*

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### *Claim Rejections - 35 USC § 112*

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 7, 9, 16, and 20 recites the limitation "RTI". There is insufficient antecedent basis for this limitation in the claim. It is unclear what "RTI" stands for or means, since it has not been defined prior to these claims.

### *Claim Rejections - 35 USC § 103*

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-7, 9-14, 16-19, and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shang et al., U.S. Patent Number 5,941,980 (herein referred to as Shang) in view of Iizuka, U.S. Patent Number 5,299,321 (herein referred to as Iizuka).

9. Referring to claim 1, Shang has taught a method of providing instructions to a processor from an emulation instruction register comprising:

a. Determining the validity of a first instruction of the plurality of instructions (Shang Abstract; column 15, lines 20-61; and Figure 2);

b. Determining the validity of a second instruction of the plurality of instructions (Shang Abstract; column 15, lines 20-61; and Figure 2); and

10. Shang has not explicitly taught:

a. Receiving a plurality of instructions simultaneously from the emulation instruction register;

b. Providing the first instruction of the plurality of instructions to a decoder if the first instruction is valid;

c. Providing the second instruction of the plurality of instructions to the decoder if the second instruction is valid.

11. However, Shang has taught use in a superscalar processor (Shang column 2, lines 45-54). Iizuka has taught the details of a VLIW superscalar processor (Iizuka column 1, lines 23-34) comprising:

a. Receiving a plurality of instructions simultaneously from the emulation instruction register (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4);

b. Providing the first instruction of the plurality of instructions to a decoder (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4) if the first instruction is valid (Shang Abstract; column 15, lines 20-61; and Figure 2);

c. Providing the second instruction of the plurality of instructions to the decoder (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4) if the second instruction is valid (Shang Abstract; column 15, lines 20-61; and Figure 2).

12. A person of ordinary skill at the time the invention was made would have recognized that the details of the superscalar processor allow for instructions to be executed in parallel to increase processor efficiency and speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the superscalar processor details of Iizuka in the device of Shang to improve processor efficiency and speed.

13. Referring to claim 2, Shang has taught determining the size of the plurality of instructions (Shang Abstract; column 15, lines 20-61; and Figure 2). In regards to Shang, the instruction size

is needed in order to determine where the next instruction begins (Shang column 4, line 63 to column 5, line 7).

14. Referring to claim 3, Shang has not explicitly taught storing the plurality of instructions in a single instruction register. However, Shang has taught use in a superscalar processor (Shang column 2, lines 45-54). Iizuka has taught the details of a VLIW superscalar processor (Iizuka column 1, lines 23-34) including storing the plurality of. instructions in a single instruction register (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4). A person of ordinary skill at the time the invention was made would have recognized that the details of the superscalar processor allow for instructions to be executed in parallel to increase processor efficiency and speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the superscalar processor details of Iizuka in the device of Shang to improve processor efficiency and speed.

15. Referring to claim 4, Shang has taught loading the second instruction of the plurality of instructions after determining the first instruction is invalid (Shang Abstract; column 15, lines 20-61; and Figure 2).

16. Referring to claims 5 and 6, Shang has not explicitly taught:

a. Loading the plurality of instructions in parallel into the emulation instruction register (Applicant's claim 5) and

b. Providing the second instruction to the decoder after the first instruction is completed (Applicant's claim 6).

17. However, Shang has taught use in a superscalar processor (Shang column 2, lines 45-54). Iizuka has taught the details of a VLIW superscalar processor (Iizuka column 1, lines 23-34) including:

a. Loading the plurality of instructions in parallel into the emulation instruction register (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4) and

b. Providing the second instruction to the decoder after the first instruction is completed (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4).

18. A person of ordinary skill at the time the invention was made would have recognized that the details of the superscalar processor allow for instructions to be executed in parallel to increase processor efficiency and speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the superscalar processor details of Iizuka in the device of Shang to improve processor efficiency and speed.

19. Referring to claim 7, Shang has taught providing the plurality of instructions to the decoder without receiving multiple RTIs (Shang Abstract; column 15, lines 20-61; and Figure 1).

20. Referring to claims 9 and 10, Shang has taught a method of processing instructions within a processor comprising receiving an RTI (Shang Abstract; column 1, lines 20-61; and Figure 2). Shang has not explicitly taught:

a. Loading a plurality of instructions into a single instruction register (Applicant's claim 9);

b. Simultaneously providing the plurality of instructions to the processor (Applicant's claim 9); and

c. Processing the plurality of instructions (Applicant's claim 9).

d. Loading the plurality of instruction into an N-bit emulation instruction register (Applicant's claim 10).

21. However, Shang has taught use in a superscalar processor (Shang column 2, lines 45-54). Iizuka has taught the details of a VLIW superscalar processor (Iizuka column 1, lines 23-34) comprising:

a. Loading a plurality of instructions into a single instruction register (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4);

b. Simultaneously providing the plurality of instructions to the processor (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4); and

c. Processing the plurality of instructions (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4).

d. Loading the plurality of instruction into an N-bit emulation instruction register (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4).

22. A person of ordinary skill at the time the invention was made would have recognized that the details of the superscalar processor allow for instructions to be executed in parallel to

increase processor efficiency and speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the superscalar processor details of Iizuka in the device of Shang to improve processor efficiency and speed.

23. Referring to claim 11, Shang has taught determining the validity of each of the plurality of instructions before processing (Shang Abstract; column 15, lines 20-61; and Figure 2).

24. Referring to claim 12, Shang has taught aborting the processing of any invalid instructions and loading a next instruction of the plurality of instructions (Shang Abstract; column 15, lines 20-61; and Figure 2).

25. Referring to claim 13, Shang has taught loading a next instruction of the plurality of instructions if a no-operation instruction is loaded (Shang Abstract; column 15, lines 20-61; and Figure 2).

26. Referring to claim 14, Shang has taught providing the plurality of instruction to the processor a plurality of times without reloading the instruction register (Shang Abstract; column 15, lines 20-61; and Figure 2).

27. Referring to claims 16 and 17, Shang has taught a processor comprising emulation control logic adapted to control the flow of the plurality of instructions to a processor pipeline following detection of a single RTI (Shang Abstract; column 15, lines 20-61; and Figure 2). Shang has not explicitly taught:

a. An instruction register adapted to store a plurality of instructions (Applicant's claim 16),

b. A decoder which may receive the plurality of instructions for processing (Applicant's claim 16).

c. Wherein the instruction register is an emulation instruction register (Applicant's claim 17).

28. However, Shang has taught use in a superscalar processor (Shang column 2, lines 45-54). Iizuka has taught the details of a VLIW superscalar processor (Iizuka column 1, lines 23-34) comprising:

a. An instruction register adapted to store a plurality of instructions (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4),

b. A decoder which may receive the plurality of instructions for processing (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4).

c. Wherein the instruction register is an emulation instruction register (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4).

29. A person of ordinary skill at the time the invention was made would have recognized that the details of the superscalar processor allow for instructions to be executed in parallel to increase processor efficiency and speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the superscalar processor details of Iizuka in the device of Shang to improve processor efficiency and speed.

30. Referring to claim 18, Shang has taught wherein the control logic determines the validity of the plurality of instructions and discards any invalid instructions (Shang Abstract; column 15, lines 20-61; and Figure 2).

31. Referring to claim 19, Shang has taught wherein the control logic loads a next instruction immediately after detecting a no-operation instruction (Shang Abstract; column 16, lines 20-61; and Figure 2).

32. Referring to claims 21 and 22, Shang has taught an apparatus, including instructions residing on a machine-readable storage medium, for use in a machine system to handle a plurality of instructions, the instructions pausing the machine to receive and RTI (Shang Abstract; column 15, lines 20-61; and Figure 2). Shang has not explicitly taught:

a. Load the plurality of instructions into a single instruction register (Applicant's claim 21);

b. Provide the plurality of instructions to the processor (Applicant's claim 21); and

c. Process the plurality of instructions (Applicant's claim 21).

d. Wherein the instruction register is an emulation instruction register (Applicant' claim 22).

33. However, Shang has taught use in a superscalar processor (Shang column 2, lines 45-54). Iizuka has taught the details of a VLIW superscalar processor (Iizuka column 1, lines 23-34) comprising:

a. Load the plurality of instructions into a single instruction register (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4);

b. Provide the plurality of instructions to the processor (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4); and

c. Process the plurality of instructions (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4).

d. Wherein the instruction register is an emulation instruction register (Iizuka column 1, line 35 to column 2, line 42; column 3, line 61 to column 4, line 11; column 4, line 26-52; Figure 1; and Figure 4).

34. A person of ordinary skill at the time the invention was made would have recognized that the details of the superscalar processor allow for instructions to be executed in parallel to increase processor efficiency and speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the superscalar processor details of Iizuka in the device of Shang to improve processor efficiency and speed.

35. Referring to claim 23, Shang has taught wherein the validity of each of the plurality of instructions is determined before processing (Shang Abstract; column 15, lines 20-61; and Figure 2).

36. Claims 8, 15, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shang in view of Iizuka as applied to claims 1, 9, and 16 above, and further in view of Applicant's admitted prior art (herein referred to Prior Art).

37. Referring to claims 8 and 15, Shang in view of Iizuka has not explicitly taught providing instructions to a digital signal processor. However, Shang in view has taught execution units with specific purposes (Shang column 1, lines 28-33). Prior Art has taught providing instructions to a digital signal processor (Prior Art page 1, line 19 to page 2, line 2). A person of ordinary skill at the time the invention was made would have recognized that DSPs are more

efficient at processing multimedia applications. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the DSP of Prior Art in the device of Shang in view of Iizuka in order to more efficiently complete processing of multimedia applications.

38. Referring to claim 20, Shang in view of Iizuka has not explicitly taught wherein the processor is a digital signal processor. However, Shang in view has taught execution units with specific purposes (Shang column 1, lines 28-33). Prior Art has taught wherein the processor is a digital signal processor (Prior Art page 1, line 19 to page 2, line 2). A person of ordinary skill at the time the invention was made would have recognized that DSPs are more efficient at processing multimedia applications. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the DSP of Prior Art in the device of Shang in view of Iizuka in order to more efficiently complete processing of multimedia applications.

***Conclusion***

39. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Akihiro et al., EP 0417013 A2, has taught an instruction unit which determines the validity of an instruction.

b. Tremblay et al., U.S. Patent Number 6,065,108, has taught a device which determines the validity of an instruction.

40. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

41. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

42. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

September 8, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100